CLAIMS

Please cancel claims 1-3, 6-10, 13-15, 18-20, 41-43 and 45-46 without prejudice.

Claims 1-22 (Canceled)

23. (Original) A system to correct a jittered signal comprising:

a counter to receive a base signal and to output a count of the duration of the base signal;

a rising edge detector to receive the jittered signal and to output a detection of a rising edge of the jittered signal;

a falling edge detector to receive the jittered signal and to output a detection of a falling edge of the jittered signal;

a rising edge position adjuster to receive the detection of the rising edge from the rising edge detector, to receive the count from the counter, to determine a rising edge count, to determine whether the rising edge count is within a programmed rising edge window, and to output a center position of the rising edge window as a jitter corrected rising edge position;

a falling edge position adjuster to receive the detection of the falling edge from the falling edge detector, to receive the count from the counter, to determine a falling edge count, to determine whether the falling edge count is within a programmed falling edge window, and to output a center position of the falling edge window as a jitter corrected falling edge position;

a jitter corrected signal output device to receive the jitter corrected rising edge position from the rising edge position adjuster, to receive the jitter

corrected falling edge position from the falling edge position adjuster, and to output the jitter corrected rising and falling edges as a jitter corrected signal by using the count from the counter.

24. (Original) The system of Claim 23, wherein the rising edge position adjuster is further configured to set the center of the rising edge window to the position of the rising edge count and to output the center of the rising edge window as the jitter corrected rising edge position if the rising edge count is outside of the programmed window of the rising edge position adjuster.

25. (Original) The system of Claim 23, wherein the jittered signal comprises an Hsync signal.

26. (Original) The system of Claim 23, wherein the base signal comprises a data enable signal.

27. (Original) The system of Claim 23 further comprising a periodic signal continuation device coupled to receive a count from the counter, wherein

the counter is configured to count during vertical blanking,

the periodic signal continuation device is configured to output to the counter a total periodic count, and

the counter is configured to reset the count after reaching the total periodic count.

28. (Original) A system to correct a jittered signal comprising:

a counter to receive a base signal and to output a count of the duration of the base signal;

a rising edge corrector to receive the jittered signal, to receive the count from the counter, to determine a rising edge count, to output the rising edge count as a jitter corrected rising edge position of the jittered signal if the rising edge count is not within a rising edge programmed window, and to output the center of the rising edge programmed window as the jitter corrected rising edge position of the jittered signal if the rising edge count is within the rising edge programmed window;

a falling edge corrector to receive the jittered signal, to receive the count from the counter, to determine a falling edge count, to output the falling edge count as the jitter corrected falling edge position of the jittered signal if the falling edge count is not within a falling edge programmed window, and to output the center of the falling edge programmed window as the jitter corrected falling edge position of the jittered signal if the falling edge count is within the falling edge programmed window; and

a jitter corrected signal output device coupled to receive the jitter corrected rising edge position from the rising edge corrector, to receive the jitter corrected falling edge position from the falling edge corrector, and to output a jitter corrected signal.

29. (Original) The system of Claim 28, wherein the jittered signal comprises an Hsync signal.

30. (Original) The system of Claim 28, wherein the base signal comprises a data enable signal.

31. (Original) The system of Claim 28 wherein the rising edge corrector further comprises:

a rising edge detector to receive the jittered signal, to detect a rising edge of the jittered signal, and

to output a rising edge detection; and a rising edge adjuster to receive the rising edge detection from the rising edge detector, to receive the count from the counter, to determine a rising edge count using the count and the rising edge detection, to output the rising edge count as the jitter corrected rising edge position if the rising edge count is not within a rising edge programmed window, and to output the center of the rising edge programmed window as the jitter corrected rising edge position of the jittered signal if the rising edge count is within the rising edge programmed window.

32. (Original) The system of Claim 28 wherein the falling edge corrector further comprises:

a falling edge detector to receive the jittered signal, to detect a falling edge of the jittered signal; and to output a falling edge detection;

a falling edge adjuster to receive the falling edge detection from the falling edge detector, to receive the count from the counter, to determine a falling edge count using the count and the falling edge detection, to output the falling edge count as the jitter corrected falling edge position if the falling edge count is not within a falling edge programmed window, and to output the center of the falling

edge programmed window as the jitter corrected falling edge position of the jittered signal if the falling edge count is within the falling edge programmed window.

33. (Original) The system of Claim 28 further comprising a periodic signal continuation device to receive the count from the counter, wherein

the counter is configured to continue to count during vertical blanking when the base signal is inactive,

the periodic signal continuation device is configured to output to the counter a total periodic count, and

the counter is configured to reset the count after reaching the total periodic count.

34. (Original) A method of correcting a jittered signal comprising:

counting a duration of a base signal;

when a rising edge of the jittered signal occurs, determining a rising edge count based on the count of the duration of the active state of the base signal;

determining whether the rising edge count is within a rising edge window;

if the rising edge count is within a rising edge window, then outputting the center of the rising edge window as a jitter corrected rising edge position or otherwise outputting the rising edge count as the jitter corrected rising edge position;

when the falling edge of the jittered signal occurs, determining a falling edge count based on the count of the duration of the active state of the base signal;

determining whether the falling edge count is within a falling edge window;

if the falling edge count is within a falling edge window, then outputting the center of the falling edge window as a jitter corrected falling edge position or otherwise outputting the falling edge count as the jitter corrected falling edge position;

outputting a jitter corrected signal by matching the count from the counter with the respective jitter corrected rising edge and falling edge positions.

35. (Original) The method of Claim 34, wherein the jittered signal comprises an Hsync signal.

36. (Original) The method of Claim 34, wherein the base signal comprises a data enable signal.

37. (Original) The method of Claim 34, further comprising:

continuing to count during an inactive state of the base signal to continue to output a jitter corrected signal;

establishing a total periodic count; and

resetting the count after reaching the total periodic count.

38. (Original) A system for reducing jitter from a first signal, wherein the system is coupled to receive the first signal and a second signal, the system comprising:

a counter to receive the second signal and to output a count related to a duration of the second signal;

a rising edge detector to receive the first signal and to output a rising edge position;

a falling edge detector to receive the first signal and to output a falling edge position;

an averager to receive the rising and falling edge positions, to average the rising and falling edge positions with previously measured rising and falling edge positions, and to output average rising and falling edge positions;

a look-up-table (LUT) device to receive the average rising and falling edge positions from the averager, to output the first signal average rising and falling edge positions as jitter corrected rising and falling edges if the rising and falling edge positions are within a programmed range of the respective average rising and falling edge positions or otherwise output the rising and falling edge positions as jitter corrected rising and falling edges;

a jitter corrected signal output device to receive the jitter corrected rising and falling edges from the LUT device and to output a jitter corrected signal.

39. (Original) The system of Claim 38, wherein the first signal comprises an Hsync signal.

Claim 38 (Canceled)

40. (Original) The system of Claim 38 further comprising a periodic signal continuation device coupled to receive the current count from the counter, wherein

the counter continues to count during vertical blanking,

the periodic signal continuation device outputs to the counter a total periodic count, and

the counter resets its count after reaching the total periodic count.

Claims 41-51 (Canceled)